

Cryptographic Engineering

Cryptography in software – the basics

Radboud University, Nijmegen, The Netherlands



Spring 2021

The software arena(s)

Embedded microcontrollers

- ▶ This is what you're looking at in the software assignment
- ▶ Typically very tight size constraints (ROM and RAM)
- ▶ Different optimization targets: size, speed
- ▶ No (or very little) parallel computation capabilities

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- ▶ Optimization target: speed (high throughput or **low latency**)
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GPUs

- ▶ Special size restrictions apply for good performance
- ▶ Optimization target: speed (**high throughput** or low latency)
- ▶ Highly parallel architectures

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 - ▶ **NOT:** $15486208/256 = 60493$ cycles for one decryption.
 - ▶ Software needs to wait until enough inputs are available
 - ▶ Delay from input to output is delay of 256 decryptions
- ▶ Highly parallel architectures (e.g., GPUs) focus on throughput
- ▶ This can be a problem for, e.g., low-latency network communication

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- ▶ For serious optimization need to count CPU cycles
- ▶ Use CPU's built-in cycle counter, e.g., on AMD64:

```
static long long cpucycles(void)
{
    unsigned long long result;
    asm volatile("rdtsc;"
                 "shlq $32,%%rdx;"
                 "orq %%rdx,%%rax"
                 : "=a" (RES)
                 :
                 : "%rdx");
    return result;
}
```

Benchmarking pitfalls

1. Your program is not running exclusively on the CPU, there may be interrupts

Solution: Measure many times, take the *median* (not average!)

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4. Getting reproducible, publicly verifiable benchmarks is hard

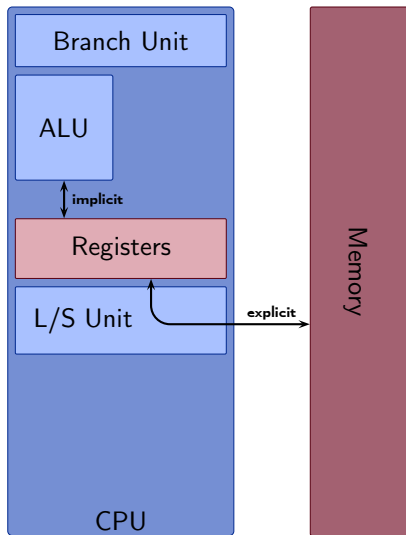
Solution: Use public benchmarking framework SUPERCOP by Bernstein and Lange:

<http://bench.cr.yp.to>

Remark: Please submit cryptographic software to eBACS!

Computers and computer programs

A highly simplified view



- ▶ A program is a sequence of *instructions*
- ▶ Load/Store instructions move data between memory and registers (processed by the L/S unit)
- ▶ Branch instructions (conditionally) jump to a position in the program
- ▶ Arithmetic instructions perform simple operations on values in registers (processed by the ALU)
- ▶ Registers are fast (fixed-size) storage units, addressed “by name”

A first program

Adding up 1000 integers

1. Set register R1 to zero
2. Set register R2 to zero
3. Load 32-bits from address $START+R2$ into register R3
4. Add 32-bit integers in R1 and R3, write the result in R1
5. Increase value in register R2 by 4
6. Compare value in register R2 to 4000
7. Goto line 3 if R2 was smaller than 4000

A first program

Adding up 1000 integers in readable syntax

```
int32 result
int32 tmp
int32 ctr

result = 0
ctr = 0
looptop:
tmp = mem32[START+ctr]
result += tmp
ctr += 4
unsigned<? ctr - 4000
goto looptop if unsigned<
```

Running the program

- ▶ Easy approach: Per “time-slot” (*cycle*) execute one instruction, then go for the next
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- ▶ This is called pipelined execution (many more stages possible)
- ▶ Advantage: cycles can be much shorter (higher *clock speed*)

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Instruction throughput and latency

- ▶ While the ALU is executing an instruction the L/S and branch units are idle

Instruction throughput and latency

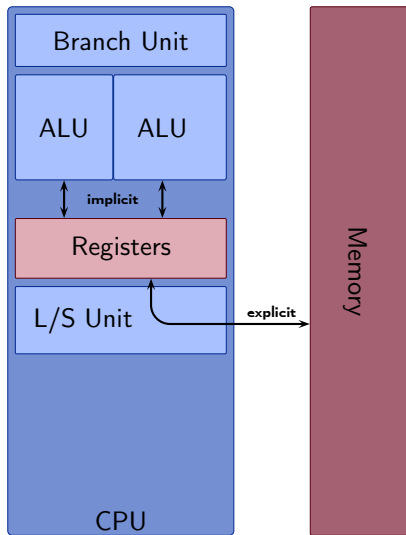
- ▶ While the ALU is executing an instruction the L/S and branch units are idle
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- ▶ While we're at it: Why not deploy two ALUs
- ▶ This concept is called *superscalar* execution

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- ▶ Idea: Duplicate fetch and decode, handle two or three instructions per cycle
- ▶ While we're at it: Why not deploy two ALUs
- ▶ This concept is called *superscalar* execution
- ▶ Number of independent instructions of one type per cycle:
throughput
- ▶ Number of cycles that need to pass before the result can be used:
latency

An example computer

Still highly simplified



Latencies and throughputs

- ▶ At most 4 instructions per cycle
- ▶ At most 1 Load/Store instruction per cycle
- ▶ At most 2 arithmetic instructions per cycle
- ▶ Arithmetic latency: 2 cycles
- ▶ Load latency: 3 cycles
- ▶ Branches have to be last instruction in a cycle

Adding up 1000 integers on this computer

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- ▶ Need at least 999 addition instructions: ≥ 500 cycles
- ▶ At least 1999 instructions: ≥ 500 cycles
- ▶ **Lower bound:** 1000 cycles

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- ▶ Comparison has to wait for addition
- ▶ Each iteration of the loop takes 8 cycles
- ▶ Total: > 8000 cycles

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- ▶ Addition has to wait for load
- ▶ Comparison has to wait for addition
- ▶ Each iteration of the loop takes 8 cycles
- ▶ Total: > 8000 cycles
- ▶ **This program sucks!**

Making the program fast

Step 1 – Unrolling

```
result = 0
tmp = mem32[START+0]
result += tmp
tmp = mem32[START+4]
result += tmp
tmp = mem32[START+8]
result += tmp

...

tmp = mem32[START+3996]
result += tmp
```

- ▶ Remove all the loop control:
unrolling

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- ▶ Remove all the loop control:
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- ▶ Each load-and-add now takes 3 cycles
- ▶ Total: ≈ 3000 cycles

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result += tmp
```

- ▶ Remove all the loop control:
unrolling
- ▶ Each load-and-add now takes 3 cycles
- ▶ Total: ≈ 3000 cycles
- ▶ Better, but still too slow

Making the program fast

Step 2 – Instruction Scheduling

```
result = mem32[START + 0]
tmp0   = mem32[START + 4]
tmp1   = mem32[START + 8]
tmp2   = mem32[START +12]
```

```
result += tmp0
tmp0 = mem32[START+16]
result += tmp1
tmp1 = mem32[START+20]
result += tmp2
tmp2 = mem32[START+24]
```

...

```
result += tmp2
tmp2 = mem32[START+3996]
result += tmp0
result += tmp1
result += tmp2
```

- ▶ Load values earlier
- ▶ Load latencies are hidden
- ▶ Use more registers for loaded values (tmp0, tmp1, tmp2)
- ▶ Get rid of one addition to zero

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- ▶ Load values earlier
- ▶ Load latencies are hidden
- ▶ Use more registers for loaded values (tmp0, tmp1, tmp2)
- ▶ Get rid of one addition to zero
- ▶ Now arithmetic latencies kick in
- ▶ Total: ≈ 2000 cycles

Making the program fast

Step 3 – More Instruction Scheduling (two accumulators)

```
result0 = mem32 [START + 0]
tmp0     = mem32 [START + 8]
result1  = mem32 [START + 4]
tmp1     = mem32 [START +12]
tmp2     = mem32 [START +16]
```

```
result0 += tmp0
tmp0 = mem32 [START+20]
result1 += tmp1
tmp1 = mem32 [START+24]
result0 += tmp2
tmp2 = mem32 [START+28]
```

...

```
result0 += tmp1
tmp1 = mem32 [START+3996]
result1 += tmp2
result0 += tmp0
result1 += tmp1
result0 += result1
```

- ▶ Use one more accumulator register (result1)
- ▶ All latencies hidden
- ▶ Total: 1004 cycles
- ▶ Asymptotically n cycles for n additions

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- ▶ Analyze the algorithm in terms of machine instructions
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- ▶ Note: Good instruction scheduling typically requires more registers
- ▶ Opposing requirements to **register allocation** (assigning registers to live variables, minimizing memory access)
- ▶ Both instruction scheduling and register allocation are NP hard
- ▶ So is the joint problem
- ▶ Many instances are efficiently solvable

Architectures and microarchitectures

What instructions and how many registers do we have?

- ▶ Instructions are defined by the **instruction set**
- ▶ Supported register names are defined by the **set of architectural registers**
- ▶ Instruction set and set of architectural registers together define the **architecture**
- ▶ Examples for architectures: x86, AMD64, ARMv6, ARMv7, UltraSPARC
- ▶ Sometimes base architectures are extended, e.g., MMX, SSE, NEON

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What determines latencies etc?

- ▶ Different **microarchitectures** implement an architecture
- ▶ Latencies and throughputs are specific to a microarchitecture
- ▶ Example: Intel Core 2 Quad Q9550 implements the AMD64 architecture

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- ▶ Harder to screw up completely

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- ▶ Information about secret data must not leak through side channels
- ▶ Most critical for software implementations on “large” CPUs: software must take constant time (independent of secret data)

Timing leakage part I

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- ▶ This code takes different amount of time, depending on s
- ▶ Obvious timing leak if s is secret
- ▶ Even if A and B take the same amount of cycles this is *generally not* constant time!
- ▶ Reasons: Branch prediction, instruction-caches
- ▶ **Never use secret-data-dependent branch conditions**

Eliminating branches

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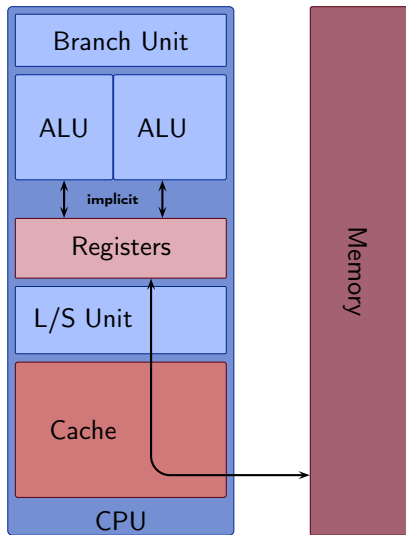
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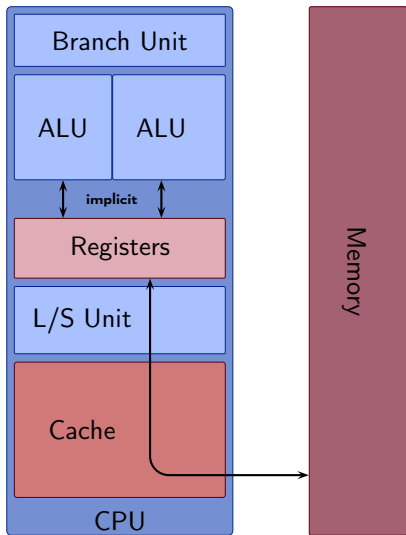
- ▶ Can expand s to all-one/all-zero mask and use XOR instead of addition, AND instead of multiplication
- ▶ For very fast A and B this can even be faster

Cached memory access



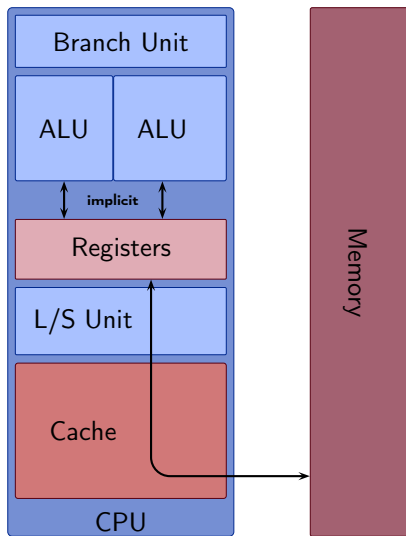
- ▶ Memory access goes through a **cache**
- ▶ Small but fast transparent memory for frequently used data

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- ▶ Small but fast transparent memory for frequently used data
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- ▶ Loading data is fast if data is in the cache (**cache hit**)
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Timing leakage part II

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- ▶ Consider lookup table of 32-bit integers
- ▶ *Cache lines* have 64 bytes
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 - ▶ Slow: cache miss (crypto just loaded from this line)

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- ▶ *Remote* timing attacks are practical:
Brumley, Tuveri, 2011: A few minutes to steal ECDSA signing key from OpenSSL implementation

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- ▶ Problem 1: if-statements are not constant time (see before)
- ▶ Problem 2: Comparisons are not constant time, replace by, e.g.:

```
static unsigned long long eq(uint32_t a, uint32_t b)  
{  
    unsigned long long t = a ^ b;  
    t = (-t) >> 63;  
    return 1-t;  
}
```

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“So the argument to the DIV instruction was smaller and DIV, on Intel, takes a variable amount of time depending on its arguments!”

—Langley, Feb. 2013

Dangerous arithmetic (examples)

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Solution

- ▶ Avoid these instructions
- ▶ Make sure that inputs to the instructions don't leak timing information

“The multicore revolution”

- ▶ Until early years 2000 each new processor generation had higher clock speeds
- ▶ Nowadays: increase performance by number of cores:
 - ▶ My laptop has 2 physical (and 4 virtual) cores
 - ▶ Smartphones typically have 2 or 4 cores
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“As a result, system designers and software engineers can no longer rely on increasing clock speed to hide software bloat. Instead, they must somehow learn to make effective use of increasing parallelism.”

—Maurice Herlihy: The Multicore Revolution, 2007

Why multicore doesn't matter...

... for algorithm design in crypto

Crypto is fast (single core of Intel Core i3-2310M)

- ▶ > 50 RSA-4096 signatures per second
- ▶ > 8000 RSA-4096 signature verifications per second
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- ▶ **Many crypto operations are trivially parallel on multiple cores**

Vector computations

Scalar computation

- ▶ Load 32-bit integer a
- ▶ Load 32-bit integer b
- ▶ Perform addition
 $c \leftarrow a + b$
- ▶ Store 32-bit integer c

Vectorized computation

- ▶ Load 4 consecutive 32-bit integers
 (a_0, a_1, a_2, a_3)
- ▶ Load 4 consecutive 32-bit integers
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Back to adding up 1000 integers

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- ▶ Need only 250 vector additions, 250 vector loads (+ adding up 4 partial sums)
- ▶ Lower bound of 250 cycles
- ▶ Very straight-forward modification of the program
- ▶ Fully unrolled loop needs only $1/4$ of the space

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- ▶ **AVX2 vector instructions are almost as fast as scalar instructions but do $8 \times$ the work**
- ▶ Situation on other architectures/microarchitectures is similar
- ▶ Reason: cheap way to increase arithmetic throughput (less decoding, address computation, etc.)

More reasons for using vector arithmetic

- ▶ Data-dependent branches are expensive in SIMD
- ▶ Variably indexed loads (lookups) into vectors are expensive
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- ▶ Need to rewrite algorithms to eliminate branches and lookups
- ▶ Secret-data-dependent branches and secret branch conditions are the major sources of timing-attack vulnerabilities
- ▶ Strong synergies between speeding up code with vector instructions and protecting code!

Vectorization problems I

Carry handling

- ▶ When adding two 32-bit integers, the result may have 33 bits (32-bit result + carry)
- ▶ Scalar additions keep the carry in a special *flag register*
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- ▶ How about carries of vector additions?
 - ▶ Answer 1: Special “carry generate” instruction (e.g., CBE-SPU)
 - ▶ Answer 2: They’re lost, recomputation is expensive
- ▶ Need to *avoid carries* instead of handling them
- ▶ No problem for today’s lecture, but requires care for big-integer arithmetic

Vectorization problems II

Removing instruction-level parallelism

- ▶ If we don't vectorize we perform multiple independent instructions
- ▶ We turn *data-level parallelism (DLP)* into *instruction-level parallelism (ILP)*

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- ▶ Pipelined and multiscalar execution need ILP
- ▶ Vectorization removes ILP
- ▶ Problematic for algorithms with, e.g., 4-way DLP
- ▶ Good example to see this: ChaCha vs. Blake
- ▶ Vectorization of ChaCha can resort to higher-level parallelism (multiple blocks)
- ▶ Harder for Blake: each block depends on the previous one

Vectorization problems III

Data shuffling

- ▶ Consider multiplication of 4-coefficient polynomials

$$f = f_0 + f_1x + f_2x^2 + f_3x^3 \text{ and } g = g_0 + g_1x + g_2x^2 + g_3x^3:$$

$$r_0 = f_0g_0$$

$$r_1 = f_0g_1 + f_1g_0$$

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$$r_3 = f_0g_3 + f_1g_2 + f_2g_1 + f_3g_0$$

$$r_4 = f_1g_3 + f_2g_2 + f_3g_1$$

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- ▶ Ignore carries, overflows etc. for a moment
- ▶ 16 multiplications, 9 additions
- ▶ How to vectorize multiplications?

Vectorization problems III

Data shuffling

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$$r_1 = f_0g_1 + f_1g_0$$

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- ▶ Can easily load (f_0, f_1, f_2, f_3) and (g_0, g_1, g_2, g_3)
- ▶ Multiply, obtain $(f_0g_0, f_1g_1, f_2g_2, f_3g_3)$

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- ▶ Multiply, obtain $(f_0g_0, f_1g_1, f_2g_2, f_3g_3)$
- ▶ And now what?

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$$r_6 = f_3g_3$$

- ▶ Can easily load (f_0, f_1, f_2, f_3) and (g_0, g_1, g_2, g_3)
- ▶ Multiply, obtain $(f_0g_0, f_1g_1, f_2g_2, f_3g_3)$
- ▶ And now what?
- ▶ Answer: Need to *shuffle* data in input and output registers
- ▶ Significant overhead, not clear that vectorization speeds up computation!

Efficient vectorization

- ▶ Most important question: Where does the parallelism come from?
- ▶ Easiest answer: Consider multiple batched encryptions, decryptions, signature computations, verifications, etc. (but that increases latency)

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- ▶ Often: Can exploit lower-level parallelism
- ▶ Rule of thumb: parallelize on an as high as possible level
- ▶ Vectorization is hard to do as “add-on” optimization
- ▶ Reconsider algorithms and data structures, synergy with constant-time algorithms

Bitslicing

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- ▶ Perform the simulated hardware implementations on many independent data streams
- ▶ Bitslicing works for every algorithm
- ▶ Bitslicing is inherently protected against timing attacks
- ▶ Efficient bitslicing needs a huge amount of data-level parallelism

Bitslicing binary polynomials

4-coefficient binary polynomials

$(a_3x^3 + a_2x^2 + a_1x + a_0)$, with $a_i \in \{0, 1\}$

4-coefficient bitsliced binary polynomials

```
typedef unsigned char poly4; /* 4 coefficients in the low 4 bits */  
typedef unsigned long long poly4x64[4];
```

```
void poly4_bitslice(poly4x64 r, const poly4 x[64])  
{  
    int i,j;  
    for(i=0;i<4;i++)  
    {  
        r[i] = 0;  
        for(j=0;j<64;j++)  
            r[i] |= (unsigned long long)(1 & (x[j] >> i))<<j;  
    }  
}
```

Bitsliced binary-polynomial multiplication

```
typedef unsigned long long poly4x64[4];
typedef unsigned long long poly7x64[7];

void poly4x64_mul(poly7x64 r, const poly4x64 a, const poly4x64 b)
{
    r[0] = a[0] & b[0];
    r[1] = (a[0] & b[1]) ^ (a[1] & b[0]);
    r[2] = (a[0] & b[2]) ^ (a[1] & b[1]) ^ (a[2] & b[0]);
    r[3] = (a[0] & b[3]) ^ (a[1] & b[2]) ^ (a[2] & b[1]) ^ (a[3] & b[0]);
    r[4] = (a[1] & b[3]) ^ (a[2] & b[2]) ^ (a[3] & b[1]);
    r[5] = (a[2] & b[3]) ^ (a[3] & b[2]);
    r[6] = (a[3] & b[3]);
}
```

Bitslicing issues

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- ▶ Can be very fast for operations that are not natively supported (like arithmetic in binary fields)
- ▶ Active data set increases massively (e.g., $128\times$)
- ▶ For “normal” vector operations, register space is increased accordingly (e.g, 16 256-bit vector registers vs. 16 64-bit integer registers)
- ▶ For bitslicing: Need to fit more data into the same registers
- ▶ Typical consequence: more loads and stores (that easily become the performance bottleneck)