Optimizing crypto on embedded microcontrollers

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Outline

1. embedded microcontrollers
2. optimizing
3. crypto
Embedded microcontrollers

“A microcontroller (or MCU for microcontroller unit) is a small computer on a single integrated circuit. In modern terminology, it is a system on a chip or SoC.”

—Wikipedia
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  - Low-end M0 and M0+
  - Mid-range Cortex-M3
  - High-end Cortex-M4 and M7
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  - Low-end M0 and M0+
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  - High-end Cortex-M4 and M7
- RISC-V 32-bit MCUs (e.g., SiFive boards)
Our Target platform

- ARM Cortex-M4 on STM32F4-Discovery board
- 192KB RAM, 1MB Flash (ROM)
- Available for <40 AUD from various vendors (e.g., ebay, element14): https://au.element14.com/stmicroelectronics/stm32f407g-disc1/dev-board-foundation-line-mcu/dp/2506840
- Additionally need USB-TTL converter and mini-USB cable
#include <stdio.h>

int main(void) {
    printf("Hello World!\n");
    return 0;
}

Getting started: Hello world!
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- How would the ELF file get run?
- What is printf supposed to do?
- Should we even expect printf to work?
Fixing all of those issues: the idea

1. Install a cross compiler: `apt install gcc-arm-none-eabi`
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9. Push “Reset” button to re-run the program
Good news! Most of that work is already done.

https://github.com/joostrijneveld/STM32-getting-started
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- Includes examples for
  - Unidirectional communication (“Hello World!”)
  - Bidirectional communication (echo)
  - Direct Memory Access
  - performance benchmarking
  - calling a function written in assembly
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  - Bidirectional communication (echo)
  - Direct Memory Access
  - performance benchmarking
  - calling a function written in assembly
- Requires python and python-serial packages
Before we optimize: how do we benchmark?

```c
SCS_DEMCR |= SCS_DEMCR_TRCENA;
DWT_CYCCNT = 0;
DWT_CTRL |= DWT_CTRL_CYCCNTENA;

int i;
unsigned int oldcount = DWT_CYCCNT;

/* Your code goes here */

unsigned int newcount = DWT_CYCCNT;

unsigned int cycles = newcount - oldcount;
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- See `cyclecount.c` example in STM32-Getting-Started
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- Caveats:
  - At >24 MHz wait cycles introduced by memory controller
  - Cycle counter overflows after ≈3 min (20 MHz)
Optimizing

- Optimize software on the assembly level
  - Crypto is worth the effort for better performance
  - Also, no compiler to introduce, e.g. side-channel leaks
  - It’s fun
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  - It’s fun

- Different from optimizing on “large” processors:
  - Size matters! (RAM and ROM)
  - Less parallelism (no vector units, not superscalar)
  - Often critical: reduce number of loads/stores
Cortex-M4 assembly basics

- 16 registers, r0 to r15
- 32 bits wide
- Not all can be used freely
  - r13 is sp, stack pointer (don't misuse!)
  - r14 is lr, link register (can be used)
  - r15 is pc, program counter
- Some status registers for, e.g., flags (carry, zero, ...)

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  - add r2, r0, r1 (three operands)
  - mov r1, r0 (two operands)
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Details on instructions: ARMv7-M Architecture Reference Manual
https://web.eecs.umich.edu/~prabal/teaching/eecs373-f10/readings/ARMv7-M_ARM.pdf

Instruction summary and timings: Cortex-M4 Technical Reference Manual
http://infocenter.arm.com/help/topic/com.arm.doc.ddi0439b/DDI0439B_cortex_m4_r0p0_trm.pdf
A simple example

```c
uint32_t accumulate(uint32_t *array, size_t arraylen) {
    size_t i;
    uint32_t r=0;
    for(i=0;i<arraylen;i++) {
        r += array[i];
    }
    return r;
}

int main(void) {
    uint32_t array[1000], sum;
    init(array, 1000);
    sum = accumulate(array, 1000);
    printf("sum: %d\n", sum);
    return sum;
}
```
accumulate in assembly

.syntax unified
.cpu cortex-m4

.global accumulate
.type accumulate, %function
accumulate:
    mov r2, #0

loop:
    cmp r1, #0
    beq done
    ldr r3,[r0]
    add r2,r3
    add r0,#4
    sub r1,#1
    b loop

done:

    mov r0,r2
    bx lr
How fast is it?

- Arithmetic instructions cost 1 cycle
- (Single) loads cost 2 cycles
- Branches cost 1 instruction if branch is not taken
- Branches cost at least 2 cycles if branch is taken
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- The loop body should cost at least 9 cycles
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accumulate:
  mov r2, #0

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  subs r1,#1
  bmi done
  ldr r3,[r0],#4
  add r2,r3
  b loop

done:

mov r0,r2
bx lr
What did we do?

- Merge `cmp` and `sub`
- Need `subs` to set flags
- Have `ldr` auto-increase `r0`
- Total saving should be 2 cycles
- Also, code is (marginally) smaller
Speeding it up, part II

accumulate:
  push {r4-r12}
  mov r2, #0

loop1:
  subs r1,#8
  bmi done1
  ldm r0!,{r3-r10}
  add r2,r3
  ...
  add r2,r10

  b loop1

done1:
  add r1,#8

loop2:
  subs r1,#1
  bmi done2
  ldr r3,[r0],#4
  add r2,r3
  b loop2

done2:
  pop {r4-r12}
  mov r0,r2
  bx lr
What did we do?

- Use `ldm` ("load multiple") instruction
- Loading $N$ items costs only $N + 1$ cycles
- Need more registers; need to push "caller registers" to the stack (push)
- Restore caller registers at the end of the function (pop)
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- Makes code somewhat larger, various tradeoffs possible
- Lower limit is slightly above 2000 cycles
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- Lower limit is slightly above 2000 cycles
- Ideas for further speedups?
Optimizing “something” vs. optimizing crypto

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- Is optimizing crypto the same as optimizing any other software?
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- Information about secret data must not leak through side channels
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  - Can be exploited remotely
  - Can eliminate systematically through “constant-time” code
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- For today, only consider timing side-channel:
  - Can be exploited **remotely**
  - Can eliminate systematically through “constant-time” code
  - Generic techniques to write constant-time code
  - Performance penalty highly algorithm-dependent
Consider the following piece of code:

```plaintext
if s then
    r ← A
else
    r ← B
end if
```
Timing leakage part I

- Consider the following piece of code:
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- General structure of any conditional branch
- \( A \) and \( B \) can be large computations, \( r \) can be a large state
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General structure of any conditional branch

- $A$ and $B$ can be large computations, $r$ can be a large state
- This code takes different amount of time, depending on $s$
- Obvious timing leak if $s$ is secret
Consider the following piece of code:

```python
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General structure of any conditional branch

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- This code takes different amount of time, depending on $s$
- Obvious timing leak if $s$ is secret
- Even if $A$ and $B$ take the same amount of cycles this is generally not constant time!

- Reasons: Branch prediction, instruction-caches
- **Never use secret-data-dependent branch conditions**
Eliminating branches

- So, what do we do with this piece of code?

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- Replace by
  
  $$r ← sA + (1 - s)B$$
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- Can expand \( s \) to all-one/all-zero mask and use XOR instead of addition, AND instead of multiplication
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- Replace by
  
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- Can expand $s$ to all-one/all-zero mask and use XOR instead of addition, AND instead of multiplication

- For very fast $A$ and $B$ this can even be faster
How about caches?

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How about caches?

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How about caches?

“The memory system is configured during implementation and can include instruction and data caches of varying sizes.”

—ARM Cortex-M7 TRM
Timing leakage part II

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- *Cache lines* have 64 bytes
- Crypto and the attacker’s program run on the same CPU
- Tables are in cache
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- Crypto continues, loads from table again

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| \( T[64] \ldots T[79] \) | \( T[80] \ldots T[95] \) | ??? | ??? | ??? |
| \( T[160] \ldots T[175] \) | \( T[176] \ldots T[191] \) | ??? | ??? | ??? |
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- Attacker loads data:
  - Fast: cache hit (crypto did not just load from this line)

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<td>$T[64] \ldots T[79]$</td>
<td>$T[80] \ldots T[95]$</td>
</tr>
<tr>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>attacker’s data</td>
<td>?</td>
</tr>
<tr>
<td>?</td>
<td>?</td>
</tr>
<tr>
<td>$T[160] \ldots T[175]$</td>
<td>$T[176] \ldots T[191]$</td>
</tr>
<tr>
<td>$T[192] \ldots T[207]$</td>
<td>$T[208] \ldots T[223]$</td>
</tr>
<tr>
<td>?</td>
<td>?</td>
</tr>
</tbody>
</table>
Timing leakage part II

- Consider lookup table of 32-bit integers
- Cache lines have 64 bytes
- Crypto and the attacker’s program run on the same CPU
- Tables are in cache
- The attacker’s program replaces some cache lines
- Crypto continues, loads from table again
- Attacker loads data:
  - Fast: cache hit (crypto did not just load from this line)
  - Slow: cache miss (crypto just loaded from this line)
Some comments on cache-timing

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  (maybe with the exception of very low-end MCUs?)
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- *Remote* timing attacks are practical:
  Brumley, Tuveri, 2011: A few minutes to steal ECDSA signing key from OpenSSL implementation
Eliminating lookups

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- Load all items, use arithmetic to pick the right one:

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  for $i$ from 0 to $n - 1$ do
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    if $p = i$ then
      $r \leftarrow d$
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    end if
  end for
  ```
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- Problem 2: Comparisons in C may be variable time, replace by, e.g.:

  ```
  static unsigned long long eq(uint32_t a, uint32_t b)
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    unsigned long long t = a ^ b;
    t = (-t) >> 63;
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- Of course much easier: do it in assembly ;-)}
Lesson so far

- Avoid all data flow from secrets to branch conditions and memory addresses
- This can *always* be done; cost highly depends on the algorithm
Is that all? (Timing leakage part III)

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—Langley, Apr. 2010
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“So the argument to the \texttt{DIV} instruction was smaller and \texttt{DIV}, on Intel, takes a variable amount of time depending on its arguments!”

—Langley, Feb. 2013
Dangerous arithmetic (examples)

- DIV, IDIV, FDIV on pretty much all Intel/AMD CPUs
- Various math instructions on Intel/AMD CPUs (FSIN, FCOS...)
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Solution

- Avoid these instructions
- Make sure that inputs to the instructions don’t leak timing information (very tricky!)
“Homework”: Optimize ChaCha20

- Stream cipher proposed by Bernstein in 2008
- Variant of Salsa20 from the eSTREAM software portfolio
- Has a state of 64 bytes, $4 \times 4$ matrix of 32-bit words
- Generates random stream in 64-byte blocks, works on 32-bit integers
- Per block: 20 rounds; each round doing 16 add-xor-rotate sequences, such as

  ```
  a += b;
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- Strategy for optimizing on the M4
  - Write `quarterround` function in assembly
  - Merge 4 `quarterround` functions into a full round
  - Implement loop over 20 rounds in assembly
  - (Implement loop over message length in assembly)
Useful features of the M4

- 16 state words won’t fit into registers, you need the stack
  - Use `push` and `pop`
  - Can also use `ldr` and `str`, `ldm`, `stm`
  - For example: `push {r0,r1} is the same as stmdb sp!, {r0,r1}`
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  - For example: `push {r0,r1}` is the same as `stmdb sp!, {r0,r1}`
- Second input of arithmetic instructions goes through barrel shifter
- Can shift/rotate one input **for free**
- Examples:
  - `eor r0, r1, r2, lsl #2`: left-shift `r2` by 2, xor to `r1`, store result in `r0`
  - `add r2, r0, r1, ror #5`: right-rotate `r1` by 5, add to `r0`, store result in `r2`
Getting started

- Download https://cryptojedi.org/peter/data/stm32f4examples.tar.bz2
- Unpack: tar xjvf stm32f4examples.tar.bz2
- Connect STM32F4 Discovery board with Mini-USB cable
- Connect USB-TTL: RX to PA2, TX to PA3
- Open terminal, run host_unidirectional.py
- Build some project, e.g., accumulate using make
- Flash accumulate1.bin to the board:
  
  st-flash write accumulate1.bin 0x8000000

- Push “reset” button to start/restart program
- Now go for ChaCha20
pqm4: post-quantum crypto on the M4

- Joint work with Matthias Kannwischer, Joost Rijneveld, and Ko Stoffelen.
- Library and testing/benchmarking framework
- Easy to add schemes using NIST API
- Optimized SHA3 shared across primitives
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- Library and testing/benchmarking framework
- Easy to add schemes using NIST API
- Optimized SHA3 shared across primitives
- Run functional tests of all primitives and implementations:
  ```python
  python3 test.py
  ```

- Generate testvectors, compare for consistency (also with host):
  ```python
  python3 testvectors.py
  ```

- Run speed and stack benchmarks:
  ```python
  python3 benchmarks.py
  ```

- Easy to evaluate only subset of schemes, e.g.:
  ```python
  python3 test.py newhope1024cca sphincs-shake256-128s
  ```
Initial pqm4 results KEM/PKE

Classic McEliece: ✖
CRYSTALS-Kyber: ✓
FrodoKEM: ✓
KINDI: ✓
NewHope: ✓
NTRU-HRSS-KEM: ✓
NTRU Prime: ✓
Post-quantum RSA-Encryption: ✖
Ramstake: ✖ (?)
SABER: ✓
(SIKE): ✓
Initial pqm4 results signatures

- CRYSSTALS-Dilithium ✓
- GUI x
- MQDSS x(?)
- Picnic x
- Post-quantum RSA-Signature x
- qTESLA ✓
- SPHINCS+ ✓